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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,625	11/02/2001	Andrew E. Phelps	2070.004900/P6765	9969

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EXAMINER	
LOHN, JOSHUA A	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,625	PHELPS ET AL.	
	Examiner	Art Unit	
	Joshua A Lohn	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,7-11,14,15 and 18-24* is/are rejected.

7)☒ Claim(s) *3,4,6,12,13,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: SYSTEM FOR DESIGN VERIFICATION USING SELECTED STATES OF A PROCESSOR-BASED SYSTEM TO REVEAL DEFICIENCIES.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 5, 14, 15, 18, 19, and 22-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Jue et al., United States Patent number 6,611,936, filed April 28, 2000.

As per claim 1, Jue discloses a method for determining one or more error conditions in a system, comprising: operating a device in the system in a first state; modifying at least one operational characteristic of the device to operate in a second state (Jue, col. 1, lines 57-65, where the different delay values represent different operating states); and determining if an error condition occurs in the system in response to modifying the operational characteristic of the

device (Jue, col. 1, lines 57-65, where it is inherent in the act of verification that a determination is made as to whether an error condition occurs or not).

As per claim 2, Jue discloses wherein modifying the operational characteristic of the device comprises reducing the number of transactions that may be processed by the device during a preselected interval when in the second state (Jue, col. 2, lines 52-63, where a delay of any number of cycles would inherently reduce the number of transactions that may be processed during an interval, like the ten cycle interval described in col. 4, lines 31-65).

As per claim 5, Jue discloses modifying the operational characteristic of the device comprises introducing non-uniform delays into the system during the second state (Jue, col. 3, lines 19-25).

As per claim 14, Jue discloses an article comprising one or more machine-readable storage media containing instructions that when executed enable a processor to: operate a device in the system in a first state; modify at least one operational characteristic of the device to operate in a second state (Jue, col. 1, lines 57-65, where the different delay values represent different operating states); and determine if an error condition occurs in the system in response to modifying the operational characteristic of the device (Jue, col. 1, lines 57-65, where it is inherent in the act of verification that a determination is made as to whether an error condition occurs or not).

As per claim 15, Jue discloses that the instructions when executed enable the processor to reduce the number of transactions that may be processed by the device for a preselected interval during the second state (Jue, col. 2, lines 52-63, where a delay of any number of cycles would

inherently reduce the number of transactions that may be processed during an interval, like the ten cycle interval described in col. 4, lines 31-65).

As per claim 18, Jue discloses that the instructions when executed enable the processor to introduce non-uniform delays into the system during the second state (Jue, col. 3, lines 19-25).

As per claim 19, Jue discloses an apparatus, comprising: an interface (Jue, col. 2, lines 52-62, where the interface is the connection leading to the programmable delay element); and a verification module adapted to receive a control signal from the interface and to adjust an operating characteristic of the apparatus to exercise a system (Jue, col. 3, lines 19-25, where the control signal sets the delay value operating characteristic to exercise the system) in a manner that is capable of revealing one or more error conditions in the system in response to receiving the control signal (Jue, col. 1, lines 57-65, where it is inherent in the act of verification that a determination is made as to whether an error condition occurs or not).

As per claim 22, Jue discloses that the verification module reduces the number of transactions that may be processed by the apparatus for a preselected interval (Jue, col. 3, lines 19-25, where the delay is variable, and any predetermined period could see a decrease in the number of transactions due to an increase in the programmed delay size).

As per claim 23, Jue discloses that the verification module increases the number of transactions that may be processed by the apparatus for a preselected interval (Jue, col. 3, lines 19-25, where the delay is variable, and any predetermined period could see an increase in the number of transactions due to a decrease in the programmed delay size).

As per claim 24, Jue discloses that the verification module adjusts the number of responses that may be transmitted to other devices at a preselected time (Jue, col. 2, lines 45-48, where the use of a bi-directional delay system would cause a delay in the transmission of responses and result in fewer responses over a preselected time period).

Claims 7 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Kamiyama, Japanese Patent number JP 62012985 A, published January 21, 1987.

As per claim 7, Kamiyama discloses a system, comprising: a control unit adapted to provide a control signal (Kamiyama, see control circuit of abstract); a first device adapted to generate one or more requests (Kamiyama, where it is inherent that some form of device generated a storage request in order for the FIFO memory device to reach a full state, as is indicated in the abstract); and a second device adapted to process one or more requests from the first device using a first configuration and adapted to process one or more requests using a second configuration in response to receiving the control signal (Kamiyama, the FFIFO memory device processes one or more requests from the first device using a first configuration, the initial memory area size, and a second configuration, the changed memory area, is used in response to control signal provided by a FIFO memory size changing control circuit).

As per claim 8, Kamiyama discloses the second device comprises a FIFO queue, and wherein the first configuration of the second device comprises a pointer of the FIFO queue configured to a first level and the second configuration comprises the pointer of the FIFO queue pointer configured to a second level (Kamiyama, abstract, where the memory limit pointer adjusts to change the configurations).

Claims 7, 9, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Bailey et al., United States Patent number, 5,548,587, published August 20, 1996.

As per claim 7, Bailey discloses a system, comprising: a control unit adapted to provide a control signal (Bailey, col. 11, lines 50-53, where the controller is the unit responsible for adjusting the speed); a first device adapted to generate one or more requests (Bailey, col. 11, lines 46-50); and a second device adapted to process one or more requests from the first device using a first configuration and adapted to process one or more requests using a second configuration in response to receiving the control signal (Bailey, col. 11, lines 51-55, where the arbiter is the second device and the first configuration is the initial speed, and the second configuration is the speed to which the arbiter is slowed).

As per claim 9, Bailey discloses the second configuration of the second device processes the one or more requests at a slower rate than in the first configuration (Bailey, col. 11, lines 51-55, where the second configuration is the slower speed of the processing).

As per claim 10, Bailey discloses the second device comprises an arbiter that arbitrates at a preselected rate in the first configuration and at a rate slower than the preselected rate in the second configuration (Bailey, col. 11, lines 51-55).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bailey, in view of Chin et al., United States Patent Application Publication number, 2001/0010066, filed February 15, 2001. As per claim 11, Bailey discloses the system referenced by the dependence upon claim 7, however Bailey fails to disclose the use of anti-starvation logic in gaining control of the bus in the second configuration.

Chin discloses a system that provides bus access in any configuration through the use of anti-starvation logic that provides each device with access to the bus when it is not in use by any other device (Chin, paragraph 71).

It would have been obvious to one skilled in the art at the time of the invention to use the anti-starvation logic of Chin in the invention of Bailey.

This would have been obvious because Bailey provides for a basic arbiter system. Chin provides an arbiter that uses logic to ensure that no devices accessing the bus suffer starvation. It would have been obvious to avoid this starvation to allow all the devices to complete timely memory transactions (Chin, paragraph 71).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jue in view of Kamiyama. As per claim 20, Jue discloses a queue for storing entries for the testing apparatus, in the form of a FIFO array. Jue does not disclose an array with an adjustable number of entries.

Kamiyama discloses a FIFO with an adjustable number of entries (Kamiyama, abstract).

It would have been obvious to one skilled in the art at the time of the invention to include the adjustable FIFO queue of Kamiyama in the storage array of Jue.

This would have been obvious because Kamiyama discloses a memory array that can be dynamically changed in size (Kamiyama, abstract). Jue discloses the need to overwrite elements of the array when out of space, thus requiring the earliest data to be completely finished with the delay implementation (Jue, col. 4, lines 30-42). It would have been of obvious benefit to one skilled in the art at the time to implement the invention of Kamiyama in the system of Jue to allow for the dynamic expansion of the storage array to allow for more flexibility in assigning longer delays, without the worry that newly generated data slices will overwrite the old.

Claim 21 rejected under 35 U.S.C. 103(a) as being unpatentable over Jue in view of Shah, United States Patent Application Publication number US 2003/0060995 A1, filed September 17, 2001. As per claim 21, Jue fails to disclose using the verification module across a bus during an interval the bus is not in use.

Shah discloses a test circuit that utilizes an idle bus (Shah, paragraph 40).

It would have been obvious to one skilled in the art at the time for Jue to use an idle bus for verification purposes.

This would have been obvious because Jue would still have been able to perform a successful verification process, but would not have required any of the burden of an additional interface to test the system (Shah, paragraph 40).

Allowable Subject Matter

Claims 3, 4, 6, 12, 13, 16, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure is provided on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua A Lohn whose telephone number is (703) 305-3188 until October 15, 2004, at which time the number becomes (571) 272-3661. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoleil can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAL

SCOTT BADERMAN
PRIMARY EXAMINER